

Fig. 3

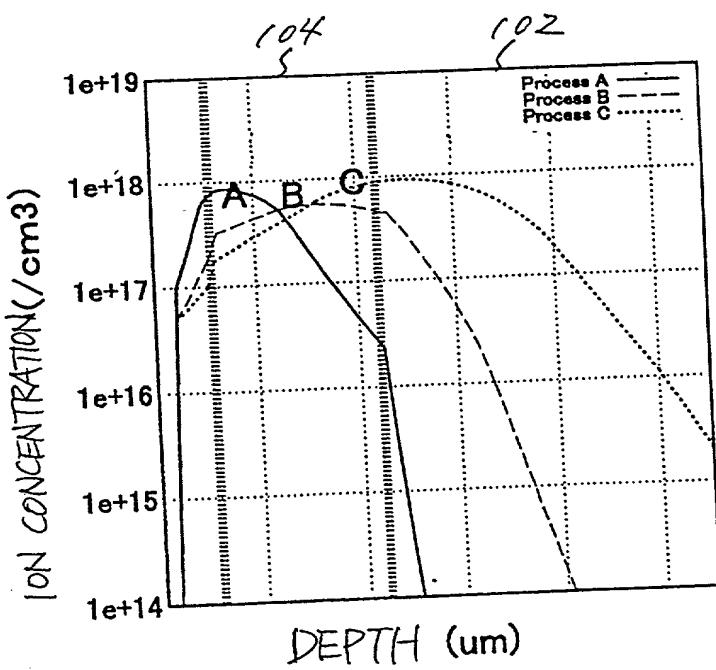


Fig. 4

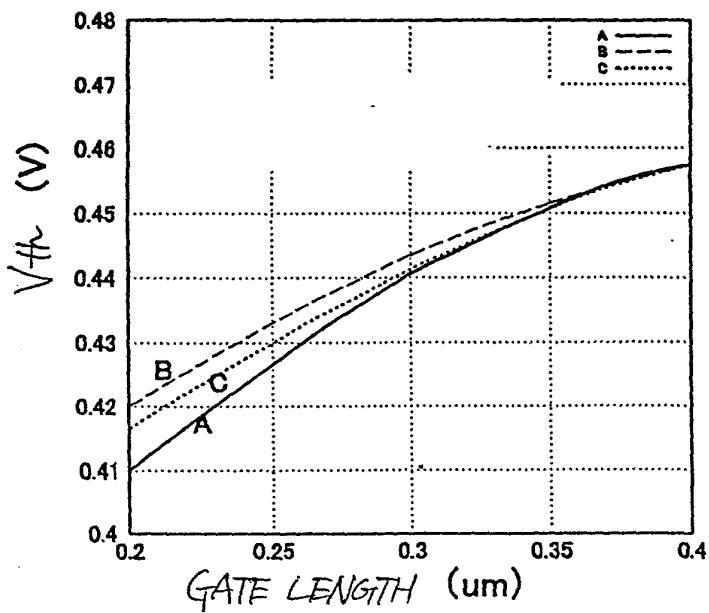


Fig-5

Fig. 6(a)

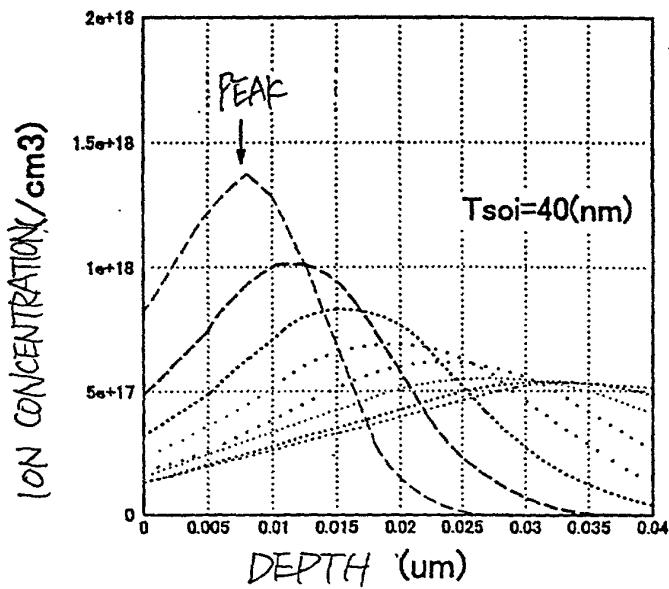


Fig. 6(b)

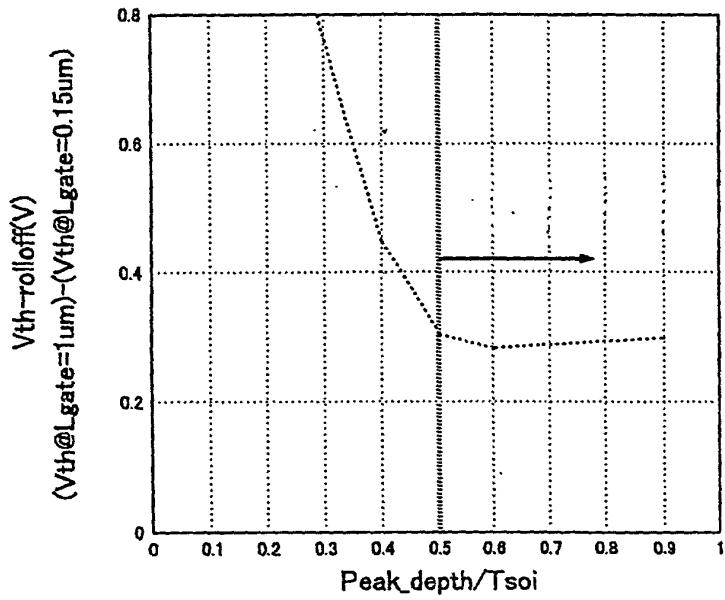


Fig. 7(a) Y[um]

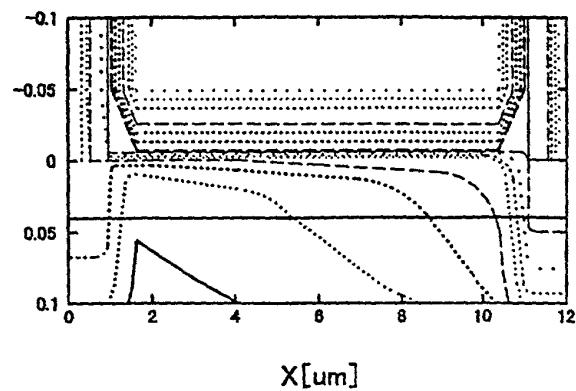
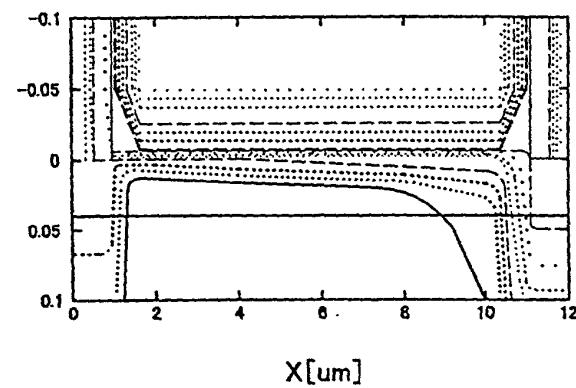
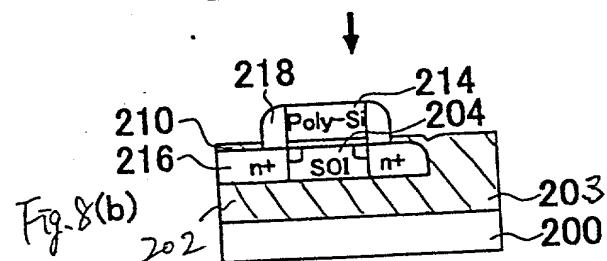
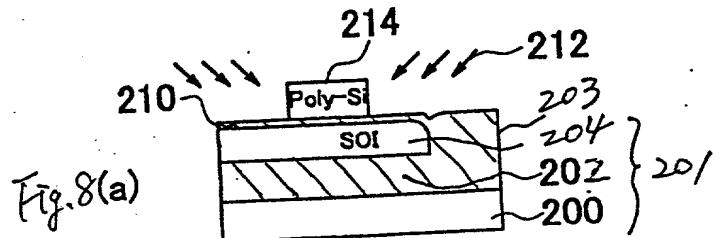
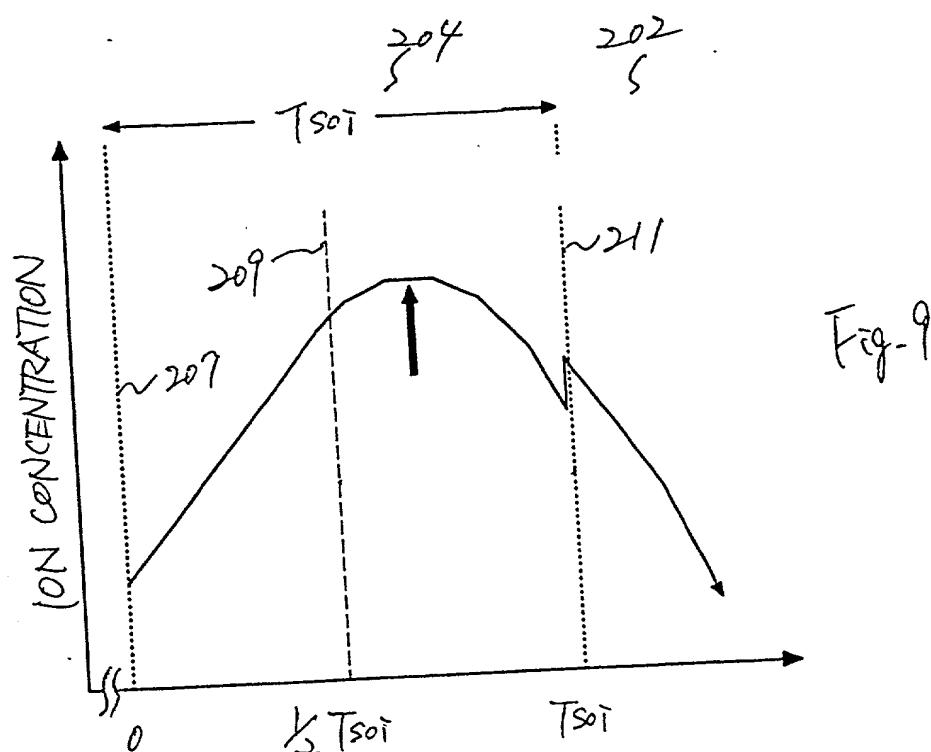


Fig. 7(b) Y[um]





POLY-SI SUBSTRATE



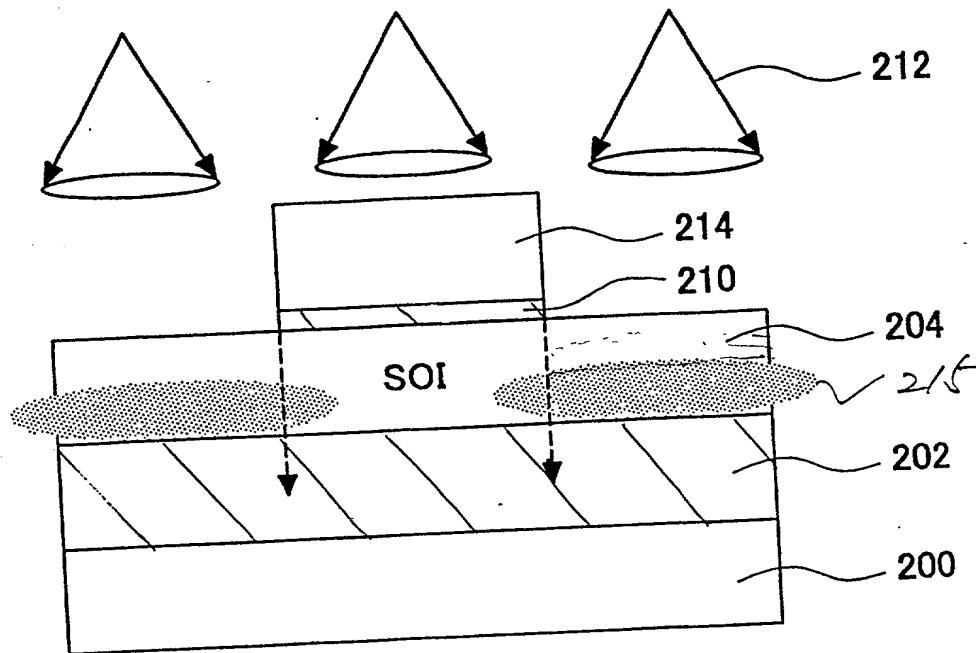


Fig-10

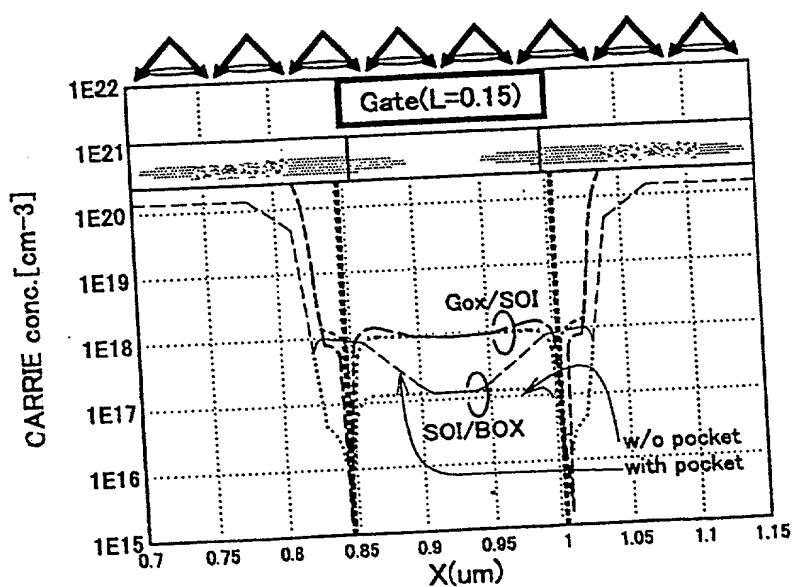


Fig-11

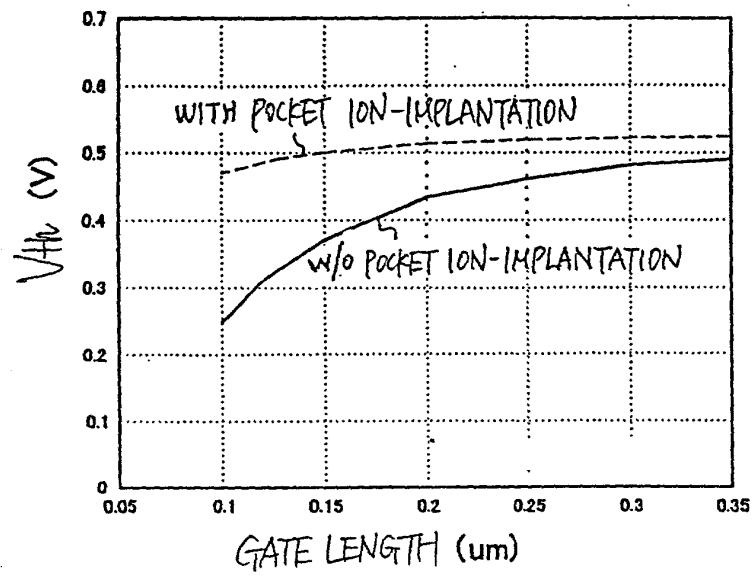
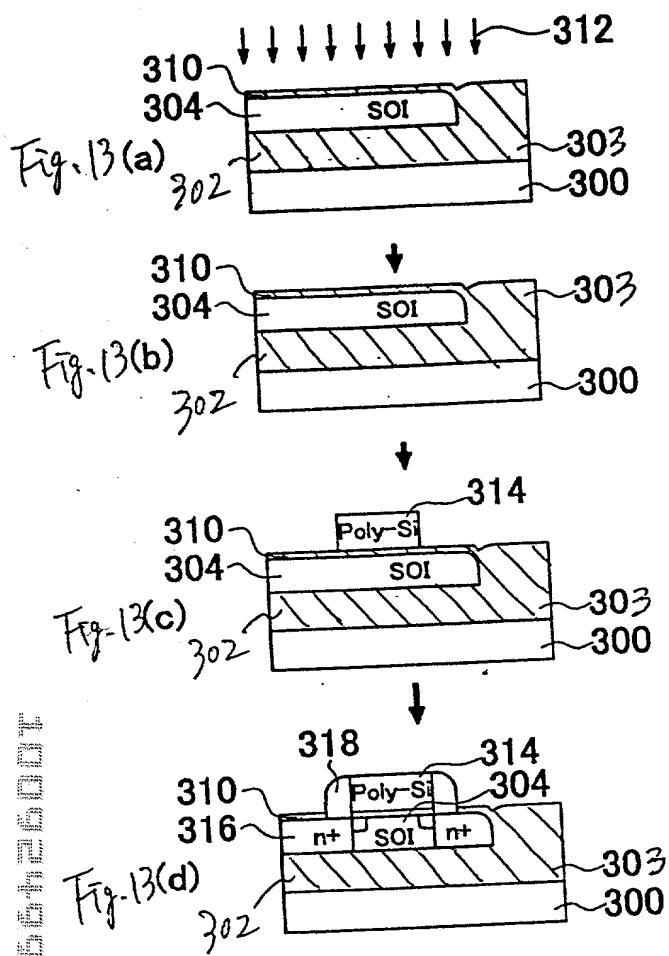


Fig-12



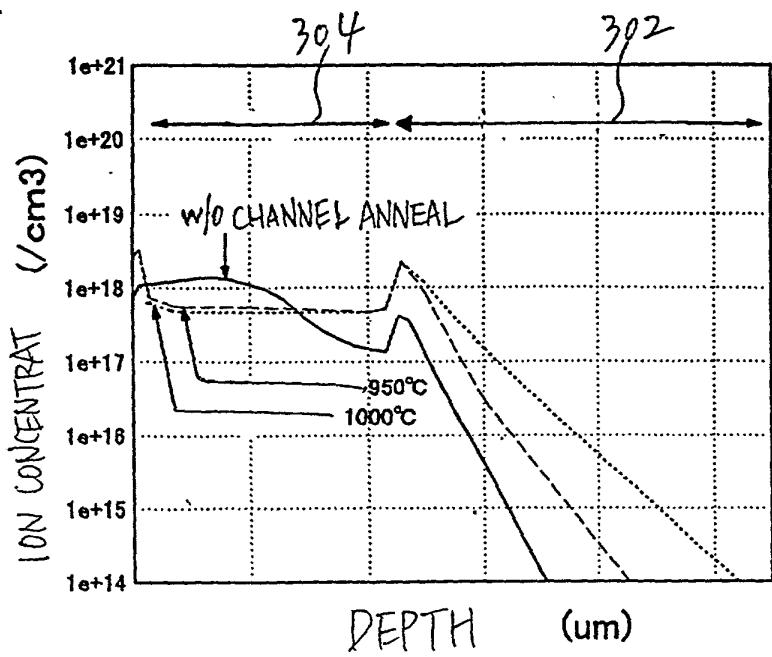


Fig. 14

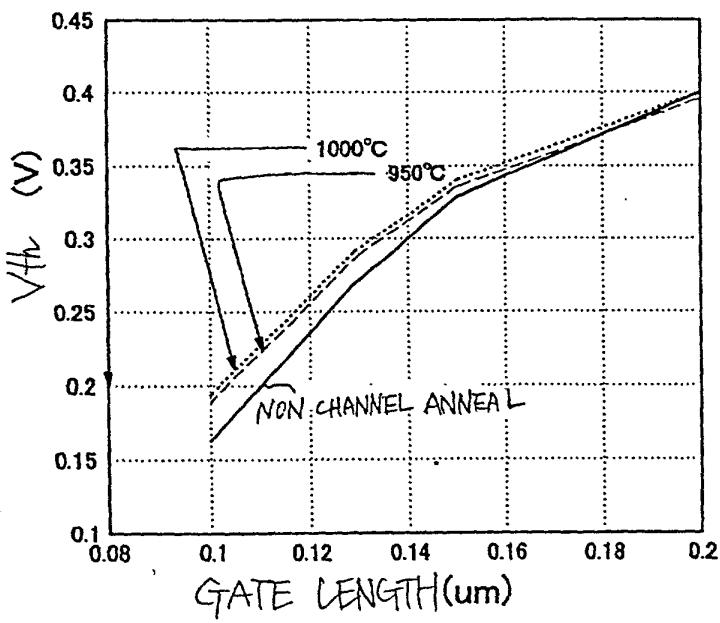
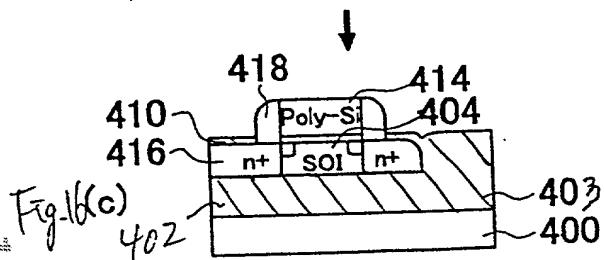
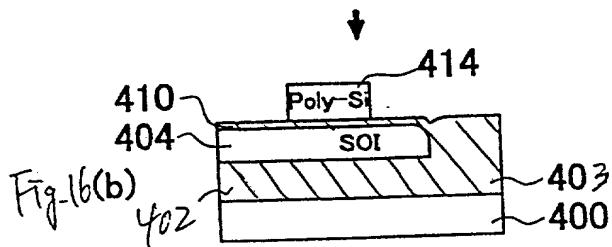
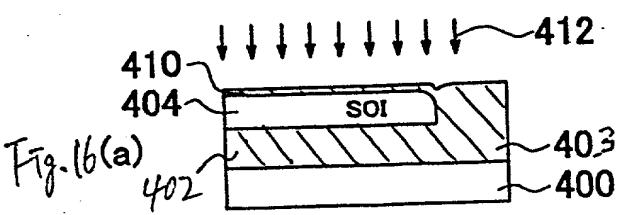


Fig. 15



PROBED D. FIGURES NOT

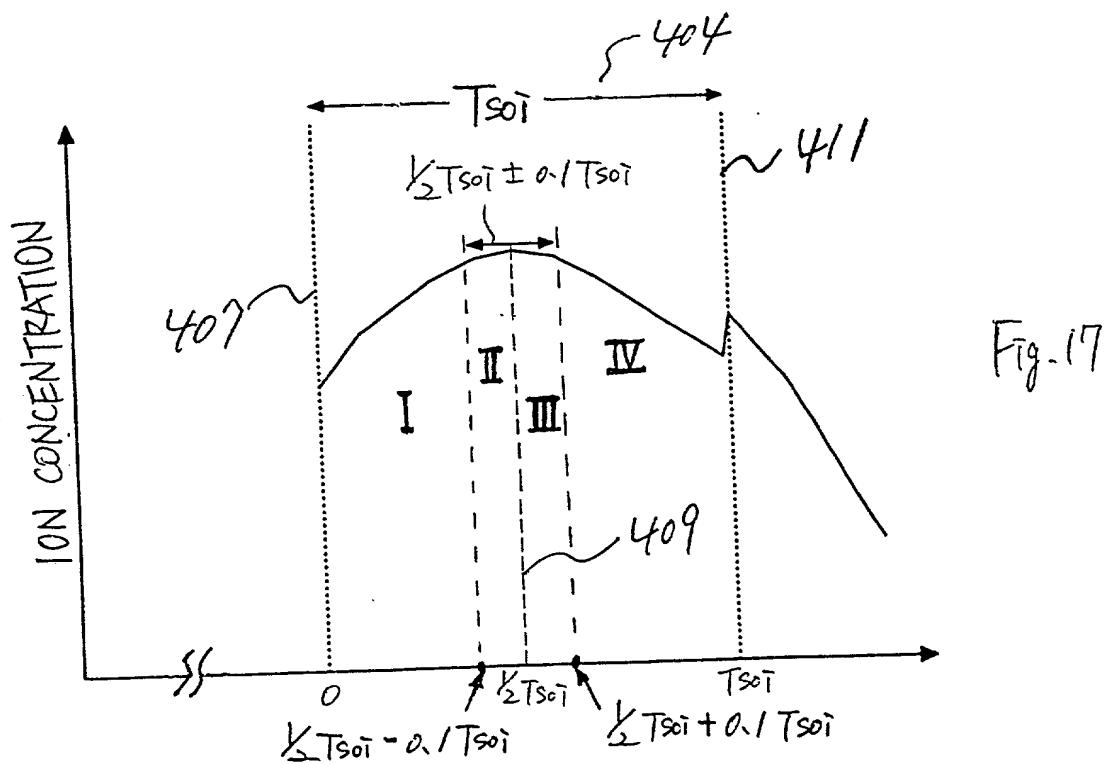


Fig. 18(a)

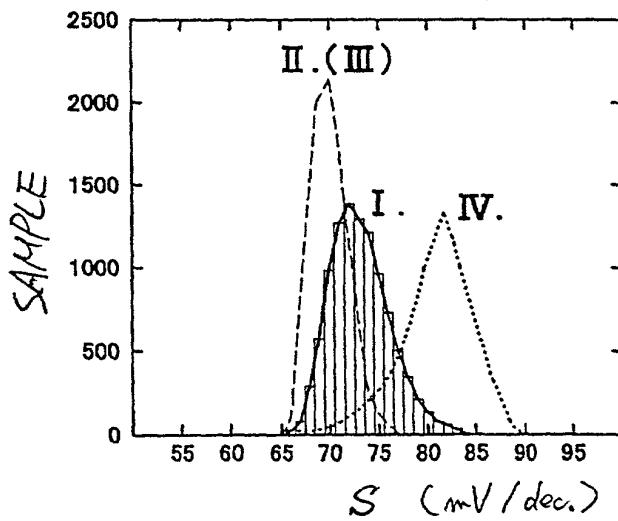
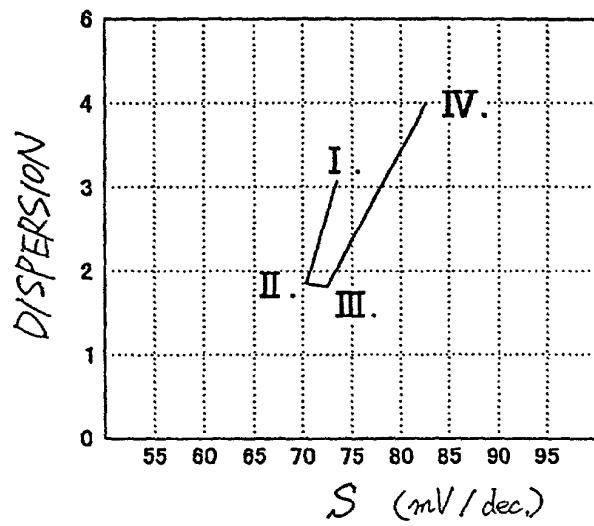


Fig. 18(b)

Fig.19(a)

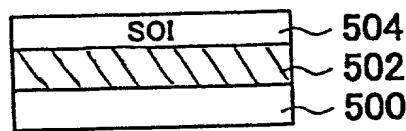


Fig.19(b)

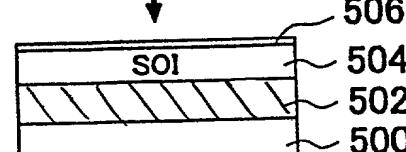


Fig.19(c)

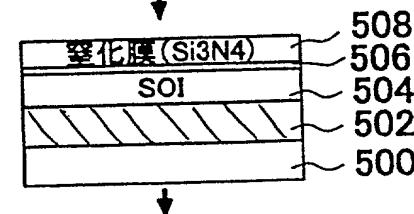


Fig.19(d)

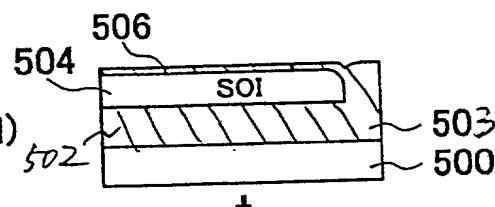


Fig.19(e)

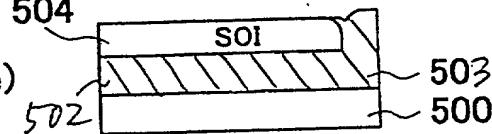
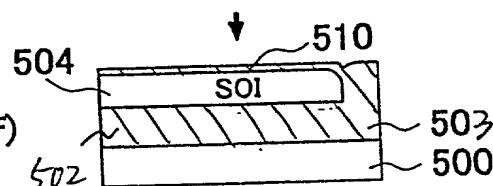
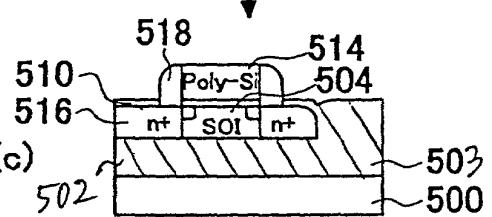
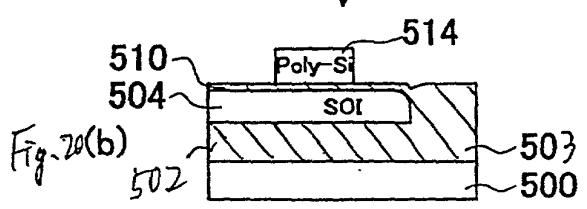
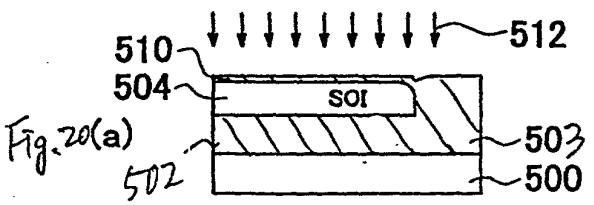


Fig.19(f)





TOSHIBA SEMICONDUCTOR

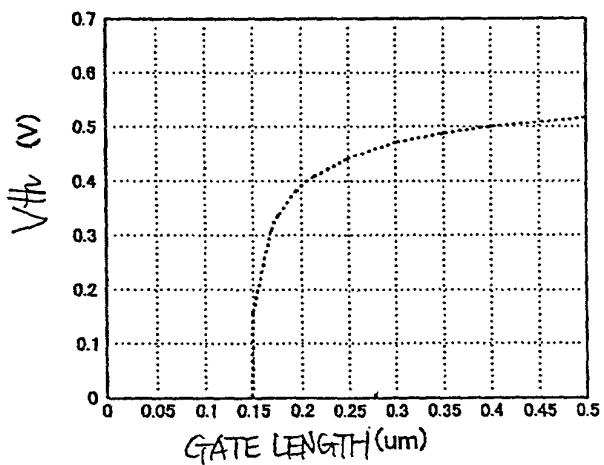


Fig. 21

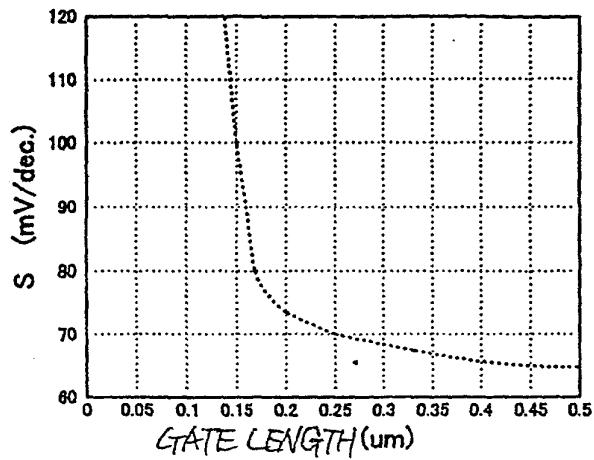


Fig-22

TABLE 15.6
Effect of Gate Length on Subthreshold Slope

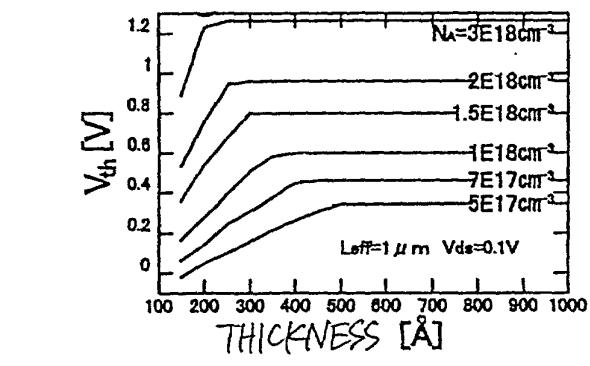


Fig-23(a)

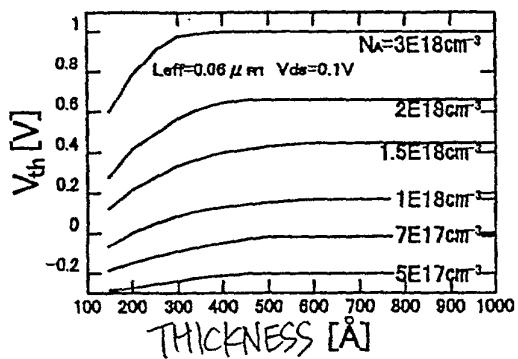


Fig-23(b)